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(54) Optical switching system.

(57) An optical switching system, wherein the input channels carrying packetized data are switched one by one at high bit rate to output channels through an optical switching network.

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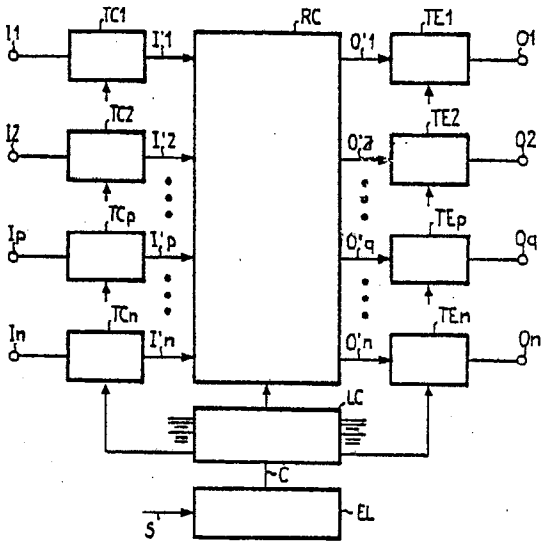

FIG. 1

EP 0 282 071 A2

Optical Switching System

The present invention concerns telecommunications systems using digital signals organized into formation blocks, the so-called packets, and more particularly it relates to an optical switching system.

Among various techniques which are presently under test for implementing broad-band telecommunications networks, asynchronous time division techniques (ATD) are of particular interest, since they are the unique networks, which, at least from a theoretical point of view, can integrate more services at different speed by an only technique. Since this technique is based upon the switching of packets with a destination label, it is also referred to as "Fast Packet Switching" or "Label Addressed Switching" technique.

Highly promising networks allowing the use of label adressed switching techniques, are described in the paper entitled "ATD Switching Networks" from Proceedings of GSLB-Seminar on Broadband Switching - Albufeira, Portugal, 19-20 January 1987, pages 225-234.

Such networks are based on small-sized switching elements (typically 2x2), organized so that the packet is self-routing through the network; each stage must examine only one bit of the label, deciding on the base of its value to which of the two outputs the packet is to be forwarded.

Since a network of this type is typically blocking, each network node needs a buffer memory, where the packet whose output is already seized by the other input can wait. As a consequence, the network is not time-transparent and its efficacy is higher if the entering traffic is randomly distributed and the ratio between presence and absence times of the signal is low. By current technologies (C-MOS) and 8 channels in parallel the global throughput of a 128x128 network can reach a few Gbit/s.

Throughput can be increased by other technologies: an order of magnitude can for instance be obtained by ECL. An alternative can be the optical technology. However, from the switching point of view, the latter technology offers the systemist rather limited performances: matrices with a small number of inputs and outputs (8x8 is already a considerable result), but with rather big size (a few cm); high input/output attenuation (some dB) and high crosstalk (few tens of dB). The most promising devices for the optical switching nowadays commercially available are based on directional couplers or on X-junctions, generally obtained by diffusing titanium optical guides in a substrate of lithium niobate. Devices with X junctions are described in the paper entitled "Survey of Optical Switching", issued on pages 143-151 of the previously-cited Proceedings, and directional couplers are described in the paper entitled "High Speed Optical Time-division and Space-division Switching" issued in the Proceedings of IOOC-ECOC 85, Venice, 1-4 October 1985, pages 81-88. Nowadays, devices of this type can allow limited-capacity matrices to be implemented (e.g. 12x12 with directional couplers, 16x16 with X-junctions). The X-junction seems to be better adapted to matrix organization, since it has no bending losses, but needs higher driving voltage.

The reduced performances of these elements are compensated for by a very large bandwidth (some tens GHz) and a quasiinfinitesimally short switching time (some tens of ps). Said characteristics render interesting the use of optical elements in the switching networks wherein the small size is normal and the bandwidth can be used to increase the ratio between presence and absence times of the signal.

So far neither optical logic devices (to be used for self-routing functions in the network) nor optical memory elements of practical use are available. Hence it does not seem that in the near future optical switching elements may be used as in electrical technology.

Therefore, a switching network based on the optical asynchronous technique needs a system organization which carries out the logic functions in the network periphery and does not require memory elements inside the network.

The optical switching system described herein solves these problems, as it allows high-speed packet-switching by means of a switching network consisting of an optical device. Negative crosstalk effects are eliminated and the network is easy to implement.

This invention consists of an optical switching system, wherein input channels carrying packetized data are switched one by one to output channels, characterized in that the packets of a generic input channel are compressed by time compressors, are converted into optical signals and, at suitable instants, are sent to an optical switching network to be switched to the desired output channel, they are then reconverted into electrical signals and expanded by time expanders to their original duration, so as to form the output channel, the switching of input channels to output channels being controlled by a centralized processor which controls the switching network through a driving circuit.

The characteristics of the invention will be clarified by the following description of an embodiment thereof, given by way of a non-limiting example, and by the enclosed drawings, where:

- Fig. 1 is a block diagram of the switching system;

- Fig.2 is a set of time diagrams of digital signals present at some points of the system;

- Fig.3 schematically represents a number of possible states of switching elements;

- Fig.4 is block diagram of the switching network;

- Fig.5 is the view of a substrate supporting the optical switching network;

- Fig. 6 is an electrical block diagram of the switching network driving circuit.

In the block diagram of Fig. 1 references I1, I2,...Ip...In and O1, O2, ...Oq...On denote inputs and outputs of the switching system, comprising time compressors TC1, TC2,...TCp...TCn and time expanders TE1, TE2,...TEq...TEn, as well as an optical switching network RC. Each block has a connection with a driving circuit LC, slaved through connection C to a centralized processor EL. The processor obtains information necessary to the system control through connection S, arriving from circuits devoted to signalling.

Let us suppose the generic input Ip activity be as represented in Fig.2, diagram Ip: namely data blocks with random arrival instants and variable durations. In this case e.g. the probability for the duration to exceed a certain value can be exponentially decreasing. Time compressor TCp function involves receiving the data block and emitting it in shorter time, as indicated in diagram I'p = O'q of Fig.2; the inverse operation is performed by the time expander TEq, whose input O'q is connected to output I'p of TCp through the optical switching network RC (Fig.1). The switching network, compressors and expanders are driven by driving circuit LC, controlled by the centralized processor EL.

The blocks re-expanded by TEq are shown in the diagram Oq of Fig.2.

Let us suppose RC network capacity be infinite and time compression/expansion be illimited, it can be stated that by increasing time compression, the probability of transit through the network of two packets at the same time can be reduced at will; practically, there is a lower boundary to such a probability, determined by the physical limits of the apparatus. However, if time compressors present also temporary-storage capability, when the network is already occupied by a data block, the others can be delayed for the necessary time; this entails no problem, since system time transparency is neither ensured, nor required. Under these conditions the network does not necessitate storage capability in its switching elements.

A network of this type can consist of elements capable of assuming two configurations, indicated by symbols "x" and "=" in Fig.3. In "x" state the two flows directly transit without interfering with each other from inputs a and b to outputs a' and b' respectively; in "=" state the outputs interchange with each other, hence inputs a and b are connected to outputs b' and a' respectively.

A network with n inputs and n outputs (nxn) is represented in Fig.4. It can consist in two columns including n switching elements each.

References X11, X12,...X1p...,X1n indicate the first column elements and X21, X22,...X2q...,X2n indicate the second column elements.

The n inputs I'1, I'2,...I'p...,I'n are connected to inputs a of n elements of the first column and the n outputs O'1, O'2,...O'q...,O'n are connected to outputs a' of n elements of the second column. Outputs a' of the elements of the first column are connected to the corresponding inputs a of elements of the second column, while per each column each output b' is connected to input b of the adjacent element.

It is finally to be noted that the elements of the second column are upside-down with respect to those of the first column.

The theoretical network capacity is at last equal to the capacity of the unique connection available, used without idle periods: 10 Gbit/s can be achieved with optical components.

Routing is performed one packet at a time with very simple rules, examining input and output indices contained in the label of the packet present at that input. If at input I'p is present a packet with output O'q, routing strategy is reduced to three cases only:

a) p<q: points X1p and X1q are activated;

b) p>q: points X2p and X2q are activated;

c) p = q: no point is activated.

After establishing the internal circuitry, high-speed packet transmission in the network is then enabled. Another connection is examined afterwards.

Even though in the present embodiment no contemporaneous connections are possible, Fig.4 shows the better clarity two connections between inputs and outputs with different order numbers: namely, with input order number inferior (I'1-O'2) and superior (I'n-O'q) to the output one.

Such a switching network can be implemented in optical technology using switching elements consisting of x junctions, which can be placed side by side on the same substrate, taking up the aspect of Fig.5.

A number n of optical parallel guides is obtained in a substrate of suitable material, e.g. by diffusing titanium in lithium niobate (LiNb03). Two more guides are obtained in the same way on the preceding at an angle equal to β and to 180-β and hence on each crosspoint metallic electrodes are deposited for applying the electrical field controlling the junction.

If angle β is small enough, $L = n^*d/\beta$, where L is minimal length of parallel optical guides, d their distance and n their number, i.e. the number of input/output lines. With L = 100 mm, d = 50 μm, and β = 0.0174 rad (1°), n is equal to 34. The distance between two following crosspoints, necessary to deposit driving electrodes, is 2.8 mm. It is worth noting that if a 100-input/output network is desired having the same physical size as that substrate, a crossing angle of 0.05 rad (2.86°), with the electrodes interspaced by 1 mm would be necessary. Said values are not compatible with the characteristics of LiNb03, but they do not seem beyond the envisaged technologic improvements attainable in the material field.

Suppose A(1) is linear guide attenuation, A(x) the attenuation of the switch element in "x" state and A(=) that in "=" state, if n is the number of inputs/outputs and L the guide length, the maximum attenuation A through the network is equal to:

$$A = 2 \bullet A(=) + (n-1)7 \bullet (x) + L \bullet A(1)$$

For the previously mentioned case (L = 100 mm, n = 30), if we suppose A(1) = 0.02 dB/mm, A-(x) = 0.15 dB and A(=) = 0.5 dB, we obtain:

$$A = 2 \bullet 0.5 + 29 \bullet 0.15 + 100 \bullet 0.02 = 7.35 \text{ dB}$$

Crosstalk at the output with the same index as the input is due to the loss of a unique X-junction in "=" state, at the other outputs it still depends on a unique junction in "x" state. A crosstalk of 25 dB, easy to discriminate from the signal, is technologically attainable for the single junction.

The block diagram of a driving circuit, particularly adapted to the switching network above, is shown in Fig. 6. It comprises the main blocks forming time compressors and driving circircuit LC of Fig.1.

It supplies a method which assigns common resources and prevents the contemporaneous access of more input signals. This method can be more or less sophisticated, adopting e.g. collision-detection multiple-access techniques or cyclic-priority systems; however, for speed and simplicity of construction a simple scanning method is to be preferred.

Data packets consisting of a variable number of octets arrive in sequence at the generic serial input Ip of Fig.6. Under the control and a centralized processor, each octet is written in the register of a FIFO memory MEp (First-In First-Out), adding a bit of presence of the datum in a suitable cell of each register. Said cells are represented dot hatched in the Figure. In correspondence with the writing of the last octet of the data packet, the signal on wire PR, belonging to connection C, is activated by the centralized processor.

A parallel-to-serial converter PSp, placed at MEp output, transforms the octets in parallel received from MEp into a serial signal with high bit-rate, which can be sent onto wire 1 to electro-optical transducer EOp. An optical fibre FOp is connected to EOp output and to the corresponding input of the already-described optical switching network.

A periodical scanning signal is sent by the processor through connection C on wire SC, connected to SET input of a SET-RESET flip-flop SRp through a four-input AND gate ASp. This signal has a period dependent on the desired transfer speed through the switching network and is phase-shifted with respect to the analogous scanning signals of the other n-1 channels by a time equal to the period divided by n. Wire BU, common to all the channels, carries a signal meaning "busy switching network" when in active state. If this signal is inactive, at the end of packet writing (active signal on wire PR) and in correspondence with the suitable time phase (active scanning signal on wire SC), the SET input of the flip-flop is enabled and its output passes to the active state. Through gate Pp also the signal on wire BU becomes active (busy switching network), that is why all the SET inputs of the other n-1 flip-flops and of the same SRp are inhibited, while RESET inputs are enabled.

The signal on wire ABp, connected to SRp output, enables in this phase the transfer of the octets from MEp, the parallel-to-serial conversion in PSp and the electro-optical conversion by EOp, which emits then a corresponding high bit-rate optical packet. The signal on wire ABp enables also the outputs of a register RIp, wherein the centralized processor has written the destination address of the channel and two bits whose active states have the meaning of p>q and p<q, q being the order number of the output Oq.

A decoder DE, common to all the channels, reads the destination address supplied by RIp on connection 2 and puts in the active state a suitable signal on one of the n output wires. In this case the active wire will be the q-th, so that the combinational circuit consisting of ORq, ADq and ACq, relative to the output, will be activated, while the combinational circuit consisting of ORp, ADp and ACp, relative to the input, will be activated by the signal on wire ABp. According to whether at register RIp output there is p<q, p>q or p=q condition on wires 3p and 4p, either gate ADp, or ACp or neither are activated, and hence through wires X1p or X2p the respective elements of the optical switching network are activated. The same occurs to output gates ADq and ACq alternatively activated by signals on wires 3q and 4q, thus through wires X1q or X2q also the output switch elements are activated.

When all the octets and corresponding presence bits have left memory MEp, the signal on wire BPp passes to inactive state, therefore the RESET

input of flip-flop SRp is activated through gate ARp and the signal indicating the switching network availability appears on wire BU.

With reference to block diagram of Fig.1, blocks TCp can be taken as consisting of blocks MEp, PSp, EOp and of optical fibre FOp of Fig.6, while all the other blocks of Fig.6 can be taken as housed in driving circuit LC of Fig.1.

Expanders TEq are easily made with circuits performing the operations inverse to those performed in the compressors.

At the output of the switching network there is an optical fibre, connected to an opto-electrical transducer, followed by a serial-to-parallel converter and by a FIFO memory, which will supply again a packet flow with the same characteristics as the input one.

Flip-flop SRp (Fig.6) still provides enabling on wire ABp.

It is clear that what described has been given only by way of non-limiting example. Variations and modifications are possible without going out of the scope of the present claims.

Claims

1. An optical switching method in a telecommunication exchange, wherein input channels carrying packetized data are switched one by one to output channels, characterized in that the packets of a generic input channel (Ip) are compressed by time compressors (TC1, ..., TCn), are converted into optical signals (by EOp) and, at suitable instants, are sent to an optical switching network (RC) to be switched to a desired output channel, they are then reconverted into electrical signals and expanded by time expanders (TE1, ..., TEn) to their original duration, so as to form the output channel (on O'q), the switching of the input channels to the output channels being controlled by a centralized processor (EL) which controls the switching network through a driving circuit (LC).

2. A system for carrying out the method of claim 1, characterized in that it comprises time compressors (TC1, ..., TCn), electro-optical and opto-electrical signal transducers (EOp), an optical switching network (RC), time expanders (TE1, ..., TEn), a centralized processor (EL) and a driving circuit (LC) between the processor (EL) and the above controlled components.

3. The system as in claim 2, characterized in that said optical switching network (RC) consists of a plurality of parallel optical guides crossed by two guides forming a small angle (β) and an angle ($180°-\beta$) supplementary to the said small angle with the parallel guides, the crosspoints being provided with electrode pairs, to which a voltage difference is applied apt to generate the desired electrical field for the deviation of the light signal from the parallel guides to the crossing ones and from the crossing ones to the parallel ones.

4. The system as in claim 2 or 3, characterized in that said time compressors (TC1, ..., TCn) comprise a FIFO memory (MEp) wherein the octets forming said packets are progressively stored at their arrival together with a presence bit and at suitable instants are sent to a parallel-to-serial converter (PSp) to be transformed into serial packets at high bit-rate and then to be transformed into optical packets by the electro-optical transducer (EOp) and sent through an optical fibre (FOp) to the switching network (RC).

5. The system as in any of claims 2 to 4, characterized in that said driving circuit (LC) comprises a decoder (DE) for decoding packet destination addresses and comprises for each input channel (I1, ..., In):

- a SET-RESET flip-flop (SRp), whose reset input is enabled by octet absence in said FIFO memory (MEp), through a presence bit (on BPp), and by a signal (on BU) with the meaning of busy switching network, while the set input is enabled by octet presence in the memory, by a signal (on PR) of packet writing end in the memory, supplied by said centralized processor (EL), by a scanning periodic signal (on SC) with a period dependent on the desired transfer speed, and by the absence of the signal (on BU) with meaning of busy switching network, the signal at the output of this flip-flop being used to enable blocks (MEp, PSp, EOp) forming the associated time compressor (TC1, ..., TCn) and time expander (TE1, ..., TEn);
- a gate (Pp), whose input is connected to the flip-flop output and whose output drives the line (BU) on which the signal relevant to switching network availability is present;
- a register (RIp), which stores the destination addresses of the packets forming the input channel and two bits (on 3p, 4p) with the meaning of order number of the input channel greater than that of the output one and vice versa under the control of said centralized processor (EL), the transfer to the output of said data being enabled by the signal at the output of the flip-flop (SRp);
- a combinational circuit (ACp, ADp, ORp), whose two outputs (X1p, X2p) are alternatively active in function of the two bits (on 3p, 4p) with the meaning of order number of the input channel greater or smaller than that of the output one, when enabled by the signal at the output of the flip-flop (SRp) or when enabled by the signal supplied by said decoder (DE), one of the two outputs being used to drive an electrode pair of said switching network.

6. The system as in any of claims 2 to 5, characterized in that said time expanders (TE1, ..., TEn) comprise an optical fibre connected to the switching network (RC), wherefrom high bit-rate packets are extracted for the opto-electrical transducer, which sends them to a serial-to-parallel converter apt to drive a FIFO memory, wherefrom the original packetized signal is extracted, the opto-electrical transducer, the serial-to-parallel converter and the FIFO memory being enabled by the signal (on ABp) supplied by said flip-flop (SRp).

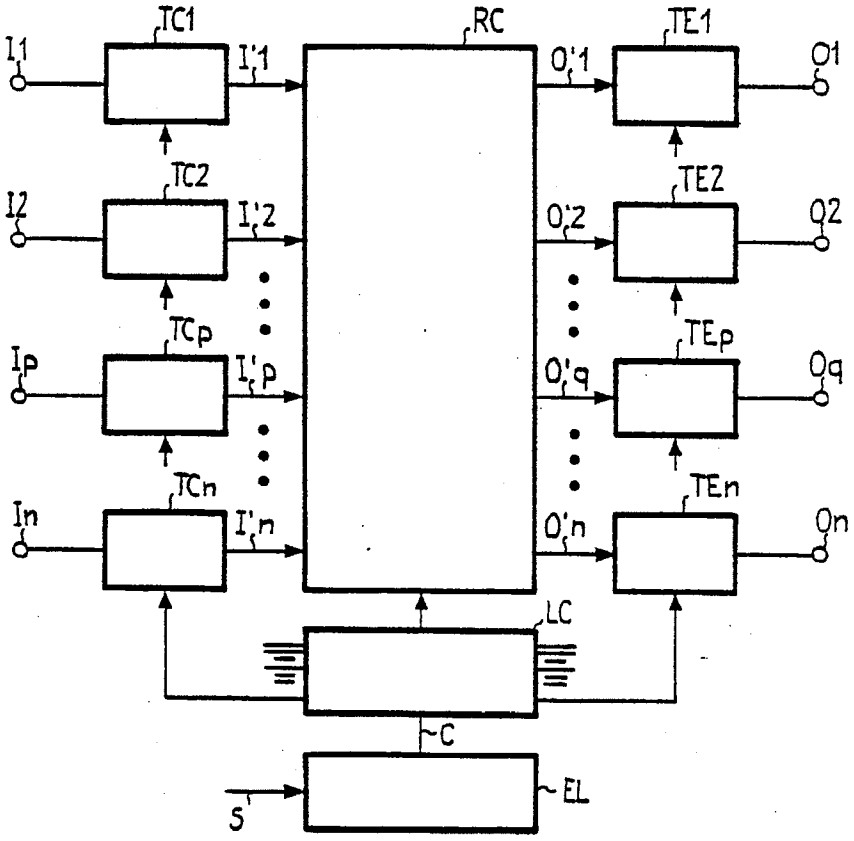
TC1
RC
TE1
I1
I'1
O'1
O1
TC2
TE2
I2
I'2
O'2
O2
TCp
TEp
Ip
I'p
O'q
Oq
TCn
TEn
In
I'n
O'n
On
LC
C
EL
S

FIG. 1

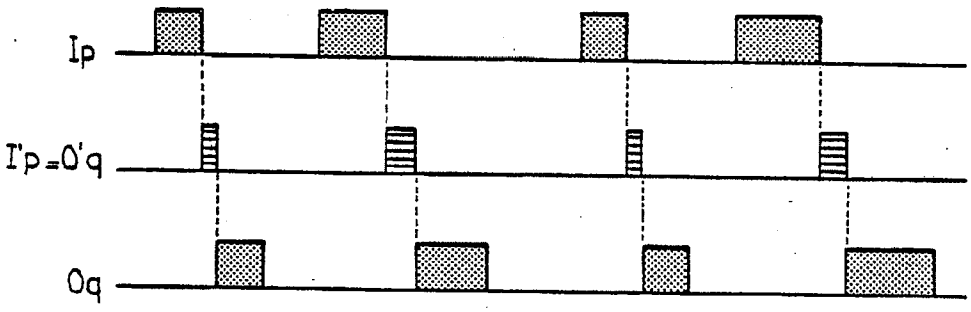
Ip
I'p=O'q
Oq

FIG. 2

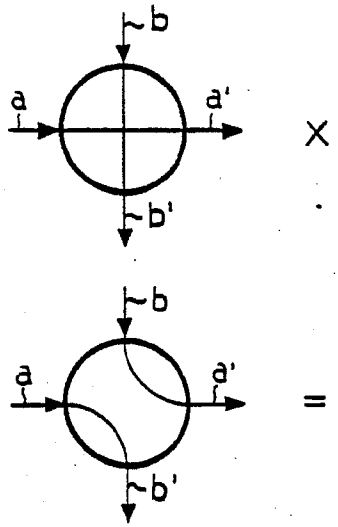
b
a
a'
b'
X
b
a
a'
b'
=

FIG. 3

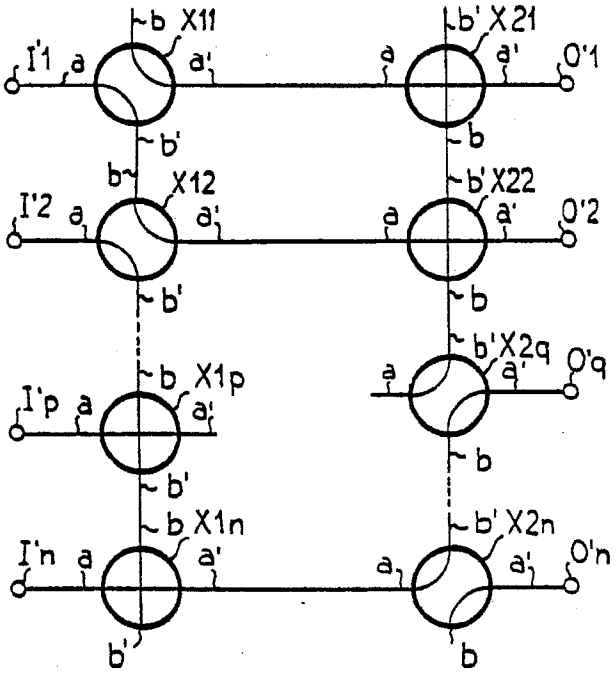
b X11
b' X21
I'1
a
a'
a
a'
O'1
b'
b
b
X12
b' X22
I'2
a
a'
a
a'
O'2
b'
b
b' X2q
b X1p
a
a'
O'q
I'p
a
a'
b'
b
b X1n
b' X2n
I'n
a
a'
a
a'
O'n
b'
b

FIG. 4

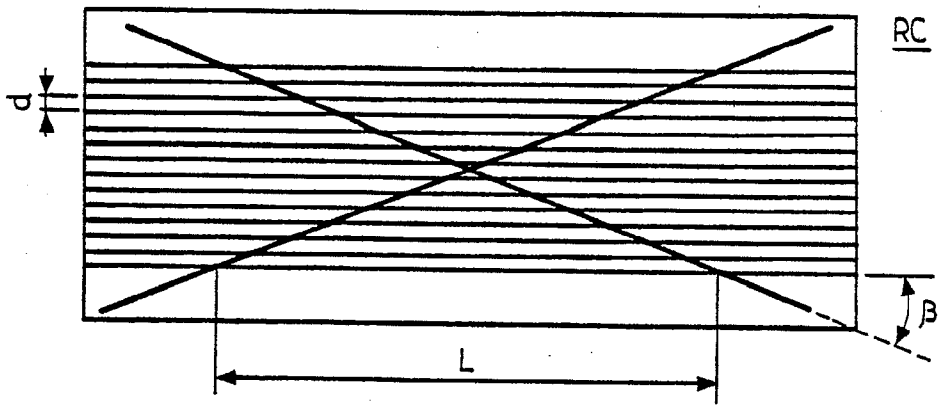
RC
d
β
L

Fig. 5

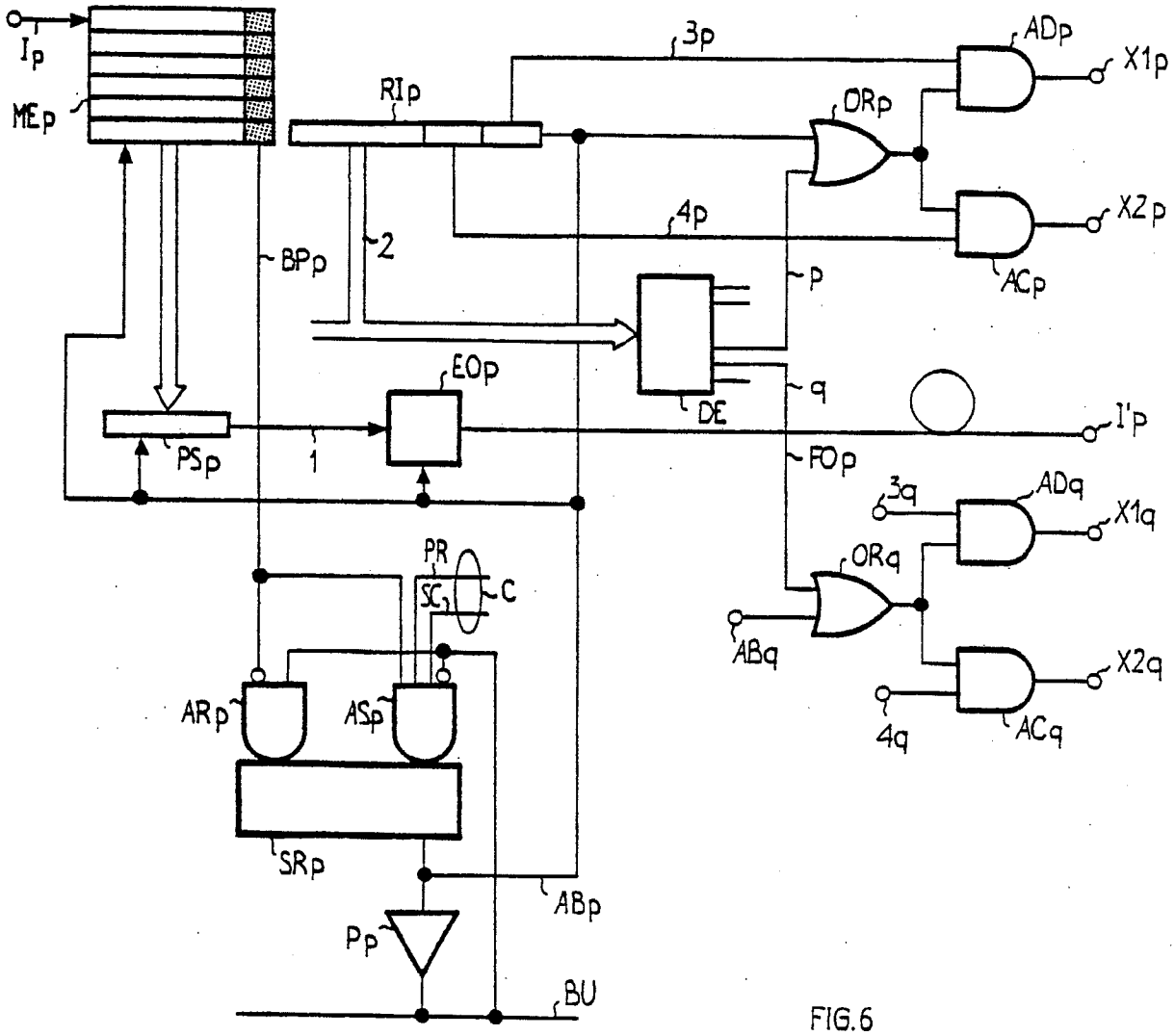
Ip
MEp
RIp
3p
ADp
X1p
ORp
4p
X2p
ACp
BPp
2
P
EOp
q
DE
I'p
PSp
1
FOp
3q
ADq
X1q
ORq
ABq
X2q
4q
ACq
PR
SC
C
ARp
ASp
SRp
ABp
Pp
BU

FIG.6

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(57) An optical switching system, wherein the input channels (I) carrying packetized data are switched one by one at high bit rate to output channels (O) through an optical switching network (RC).

The packets of a generic input channel are time compressed, converted into optical signals and, at suitable instants, sent to an optical switching network to be switched to the desired output channel, they are then reconverted into electrical signals and expanded to their original duration.

A centralized processor (EL) controls the channel switching through the switching network by means of a driving circuit (LC).

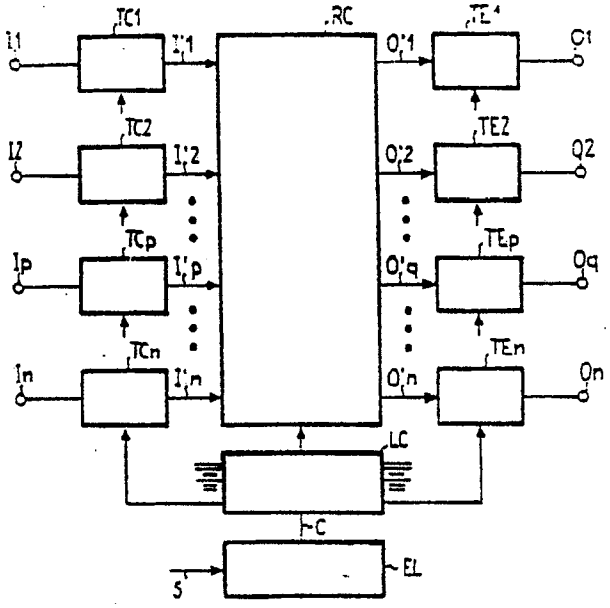

FIG. 1

EP 0 282 071 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 10 3868

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X A	GB-A-2 139 443 (S.T.C.) * Whole document *	1,2 4-6	H 04 Q 3/52 H 04 Q 11/04 H 04 L 11/20 H 04 B 9/00
P,X	PHOTONIC SWITCHING TOPICAL MEETING, Incline Village, Nevada, 18th-20th March 1987, pages 35-37, Optical Society of America, Incline Village, Nevada, US; A. DE BOSIO et al.: "Deterministic and statistic circuit assignement architectures for optical switching systems" * Whole document *	1-3	
P,A	IDEM	4,6	
A	PROCEEDINGS OF THE INTERNATIONAL SWITCHING SYMPOSIUM, Florence, 7th-11th May 1984, part 2, session 41A, paper 4, pages 1-7, Florence, IT; R.W. BLACKMORE et al.: "An opto-electronic exchange of the future" * Page 3, left-hand column, line 4 - right-hand column, line 16; figure 8 *	3	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 04 Q H 04 L G 02 F
A	US-A-4 325 147 (ROTHLAUF) * Abstract; column 1, lines 13-35; column 1, line 67 - column 2, line 29; column 3, line 66 - column 4, line 32; figure 1 *	4-6	
A	US-A-3 979 733 (FRASER) * Column 4, line 58 - column 6, line 36; figures 3,4 *	4-6	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	05-04-1989	O'REILLY D.J.K.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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